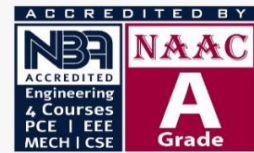




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2.2.1 MOTIVATING WEAK STUDENTS

(i) SPECIAL COACHING CLASS



JCT COLLEGE OF ENGINEERING AND TECHNOLOGY

PICHANUR, COIMBATORE - 641105



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR: 2023 - 2024 (ODD SEMESTER)

COACHING CLASS / REMEDIAL CLASS SCHEDULE

Date: 23.10.2023

This is to inform that Coaching / Remedial Class for Slow learners will be conducted in the following Day Order for III and IV Year Electronics and Communication Engineering, students from 25.10.2023 onwards (Time : 4.45 PM to 6.15 PM) till the commencement of CIA III for IV year and End Semester Examination for III Year Students are advised to co-operate for the same.

S. No.	Day	Year	Course Code / Course Name	Faculty In Charge
1	Day 1	III Year	CEC366 - Image Processing	Dr.V.J.Arulkarthick
2	Day 2		CBM370 - Wearable Devices	Prof.K.Babu
3	Day 3		EC3351 - Transmission Line and RF Systems	Prof.M.Chandrasekaran
4	Day 4		CEC352 - Satellite Communication	Prof.M.Shabana
5	Day 5		EC3552 - VLSI and Chip design	Prof.Poornima R
6	Day 6		EC3501 - Wireless Communication	Prof.A.Sindhu
7	Day 1	IV Year	EC8701 - Antennas and Microwave Engineering	Prof.M.Chandrasekaran
8	Day 2		EC8791- Embedded and Real Time Systems	Prof.S.Renswick
9	Day 3		EC8702 - Adhoc and Wireless Sensor Network.	Prof.Thahseen Thahir
10	Day 4		OBM752 - Hospital Management	Dr.V.J.Arulkarthick
11	Day 5		EC8751 - Optical Communication	Prof.Vedha Vinodha D

S. Arun
Faculty In Charge

V. J. Arulkarthick
HoD/ECE

V. J. Arulkarthick
Director IQAC




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(ii) CLASS COMMITTEE MEETING INCLUDING WEAK STUDENTS

JCT		JCT COLLEGE OF ENGINEERING AND TECHNOLOGY Pichanur, Coimbatore-641105		NAAC A	
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING					
CLASS COMMITTEE MEETING					
Academic Year : 2023 - 2024 (ODD SEMESTER)					
Class Committee Meeting No:1			Ref.No: ECE/CCM/10.11.2023		
Venue: Communication Lab			Date & Time:10.11.2023 & 2.30 PM onwards		
Chairperson-Dr.V.J.Arulkarthick HoD/ECE Faculty - 1. Prof.M.Shabana (AP/ECE) <i>Shabana</i> 2. Prof.R.Poornima (AP/ECE) <i>Poornima</i> 3. Prof .Sindhu A (AP/ECE) <i>A Sindhu</i> 4. Prof .Mohanapriya S (AP/ECE) <i>Mohanapriya</i> 5. Prof. Thahseen Thahir (AP/ECE) <i>Thahseen</i> 6. Prof.V.P.Anila (AP/CSE) <i>Anila</i> 7. Dr.S.Saravanan (AP/S & H) <i>Saravanan</i>			Class Advisor 1. Prof.Babu K (AP/ECE) <i>Babu</i> Mentor: 1. Prof.Renswick S (AP/ECE) <i>Renswick</i> 2. Prof.Mohanapriya S (AP/ECE) <i>Mohanapriya</i>		Student Representatives: 1.Arish M <i>Arish</i> 2.Gunapriya T <i>Gunapriya</i> 3.Ijas Shahadh Y <i>Ijas</i> 4.Vennapusa Abhishek Reddy <i>Abhishek</i> 5.Subramani P <i>Subramani</i>
Sl. No.	Points Discussed		Target Date	Responsibility	Remarks
1.	MA3355 Random Process and Linear Algebra - Dr.S.Saravanan (AP/S & H) <ul style="list-style-type: none">Coverage of syllabus- 2 UnitsStudents' Feed Back: Requested to Solve the home work problems in classStaff Feed Back: No Problem		-	Individual Faculty	-
2.	CS3353 C Programming and Data Structure - Prof.V.P Anila (AP/CSE) <ul style="list-style-type: none">Coverage of syllabus-1.5 UnitsStudents' Feed Back: State the real time examples to the students and elaborate them where it is appliedStaff Feed Back: No Problem		-	Individual Faculty	-



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(III) PEER GROUP LEARNING METHOD OF TEACHING



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PEDAGOGICAL INITIATIVES

Subject : EC3352 DIGITAL SYSTEM DESIGN

Year : II year

Faculty Handled: Ms.Thahseen Thahir

TOPIC	PEDAGOGICAL INITIATIVES	OBJECTIVES	SNAPSHOTS/PROOFS
HDL Models of Combinational Circuits.	Flipped Class Room	Students will be able to design and simulate combinational circuits using Hardware Description Languages (HDL) for digital system design.	https://www.youtube.com/watch?v=ccJvMFE9tul Hardware Description Language Hardware Description Language (HDL) is a language that describes the hardware of digital systems in textual form. There are two applications of HDL: prototyping. • Hardware Simulation: We use HDL programs that create a logic simulator to simulate and debug the design. The logic simulator interprets the HDL and produces a model of the hardware from the text. It will behave before it is actually fabricated. • Hardware Synthesis: The HDL programs can be compiled into the implementation using synthesizer and logic compiler tools. The output of the synthesizer is gate-level netlist, which is later used to fabricate as IC or to layout a Printed Circuit Board (PCB). There are a variety of HDLs available in the market. The most common are Verilog (based on C) and VHDL (Very High Speed Integrated Circuit Hardware Description Language) (based on Ada).
HDL Models of Registers and Counters	Flipped Class Room	Students will be able to model and implement registers and counters using HDL for sequential circuit design.	https://www.youtube.com/results?search_query=HDL+Models+of+Registers+and+Counters
Hardware Multithreading	Peer Group Learning	Students will be able to understand and apply the concept of hardware multithreading to improve the efficiency and performance of processors.	Hardware Multithreading • Allow multiple threads to share a single processor. • Requires replicating the independent state of each thread. • Virtual memory can be used to share memory among threads.
Exception handling in MIPS Architecture	Peer Group Learning	Students will be able to analyze and implement exception handling mechanisms within the MIPS architecture for effective error management.	
Introduction to Graphics Processor Units.	Peer Group Learning	Students will be able to understand the architecture and functionality of Graphics Processing Units (GPUs) and their applications in parallel processing and computing.	Introduction What is GPU? • It is a processor optimized for 2D/3D graphics, video, image processing, and similar. • It is highly parallel, highly multithreaded multi-processor designed for visual computing. • It provides real-time visual image-view with computer objects via graphics images, and videos. • It serves as both a programmable graphics processor and a reliable parallel computing platform. • Heterogeneous Systems combine a CPU with a GPU.



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IV) ASSIGNMENTS



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR: 2023 - 2024 (ODD SEMESTER)

Assignment I

Branch / Year / Semester : ECE/III/V
Course Code & Name : CBM370 & Wearable Devices

Max. Marks : 40
Submission Date : 12/09/2023

COs	Course Outcome	Knowledge Level
CO1	Summarize the concepts of wearable system.	K2
CO2	Explain the energy harvestings in wearable device	K2

Answer all the Questions (40 Marks)				
S.No.	Knowledge Level	Questions	COs	Marks
1	K2	What are the types of Wearable systems ?and explain each types.	CO1	10
2	K2	Explain the working principles of Pneumography.	CO1	10
3	K2	Summarize the concept of Plethysmography.	CO2	10
4	K2	Outline the construction and working principles of Solar Cell	CO2	10

BLOOM'S TAXANOMY LEVEL : R-REMEMBERING, U-UNDERSTANDING, AP-APPLYING,
AN-ANALYSING, E-EVALUATION, C-CREATING

B. J. Kales

Signature of the Faculty Member

V. J. Dm
HoD



Principal
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MOTIVATING BRIGHT STUDENTS

HIGHER STUDIES AND COMPETITIVE EXAMS EVENTS



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Competitive Exams

Description Links Upsc <http://www.upsc.gov.in> Gate <http://www.iitk.ac.in>

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International education expo



JCT Higher Education and Competitive Exam Guidance Cell in association with Career Zone, SI UK, Target USA -Foreign Education Partner, organized an expo for college students to study abroad. The expo was an effective platform linking prestigious foreign universities/institutions with focused overseas higher education aspirants. In around Coimbatore, Engineering College students more than 534 students [...]

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How to become an IAS



JCT Higher Education & Competitive Exam Guidance Cell has successfully organized a webinar on How to become an IAS : Preparation strategies for Union Public Services Commission Examinations (UPSC) on 20th of February 2024. One faculty from Shankar IAS Academy, an initiative of made easy group a premier institute for UPSC Civil Services Examinations helped [...]

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BEST OUTGOING STUDENT IN THE ACADEMIC YEAR 2023-2024




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